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- Baseline HBT Process Development

As described in Progress Report No. 12, a yield problem associated with the unintentional formation of a Schottky diode between the base and emitter contact resulting in low V_{be}s and low gains has been recognized. To eliminate this problem a self-aligned side wall nitride process has been developed that results in nitride being formed around the periphery of the n-ohmic and p-ohmic metal to protect the metal/GaAs interface from attack during the etch of the GaAs cap layer. Initial results obtained with this process are encouraging although it is clear that this approach does not completely eliminate the V_{be} problem. One of the advantages of this new self-aligned process is that the base-emitter turn-on voltage V_{be} and transistor gains can be measured prior to the etching of the n^+ cap layer, thus eliminating the effect of this etch on the V_{be} variations. Figure 1 shows the variation in the base-emitter turn-on voltage across a wafer for a large transistor prior to etching the cap layer. Although some variation would be expected due to variations in the cap layer doping and thickness (which should be eliminated after the cap etch), it can be seen that these variations are much greater than would be expected. Values of V_{be} greater than 0.9 V are generally associated with reasonable transistor current gains (>20), while transistors with lower V_{be}s have current gains only at very high currents. These low V_{be}s are believed to be associated with the emitter

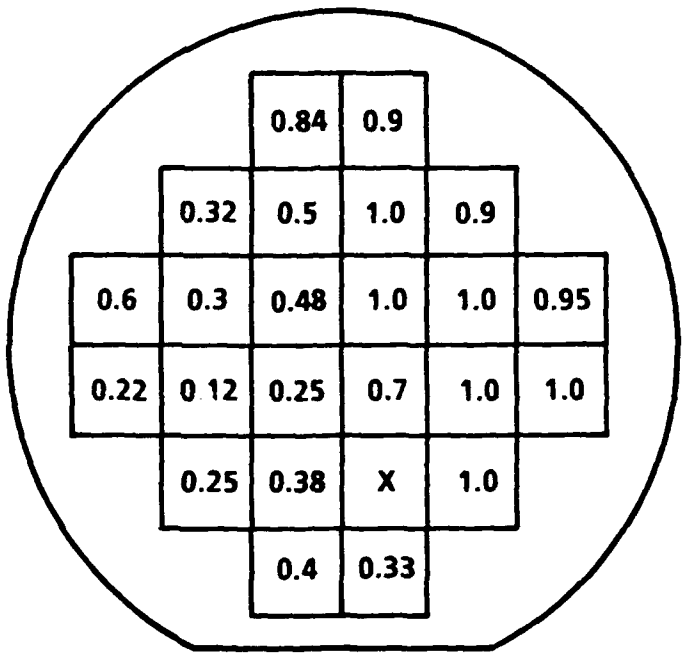

Figure 1. Wafer map showing V_{BE} variations prior to the cap etch process.

contact metal penetrating through the emitter layer and forming a Schottky diode with the underlying base layer during the 450°C n-ohmic metal sintering process.

To examine this hypothesis, the next few lots will be fabricated with the emitter cap layer thickness increased from 1000 Å to 2000 Å to prevent the penetration of the n-ohmic metal through the emitter. However, the lead ADC lot in processing has already passed the point where the emitter epi layer is deposited and will have the standard epi thickness. In addition, a parallel effort will be undertaken to improve the n-ohmic metal process to minimize the penetrations.

- Circuit Design/Testing Progress

The Hughes ADC development effort this quarter has focused on the testing of two 5-bit ADC test-bar lots from TI. Preparation for the testing effort included the design of custom wafer-level probe software, a custom thin-film hybrid, and a hybrid dynamic test fixture. As a result of wafer level testing, several functional S/H circuits have been found. However no functional 5-bit ADCs were identified. Circuit design progress consisted of a detailed architecture study of the 8-bit ADC.

In April, the test software required for the wafer level probing of the S/H circuits was completed. Test software for the 5-bit ADC was completed in the previous quarter. Also in April, fabrication of a custom thin-film hybrid required to dynamically test the 5-bit ADC and S/H circuits was completed. In addition, a dynamic test fixture that supports the custom hybrid was designed and fabricated. All the elements required for complete evaluation of the test-bar chips, from wafer level probe to high frequency dynamic test, are in place at this time.

Two 5-bit ADC test-bar lots were received from TI this quarter. The first in mid-April (lot no. 6061) and the second in mid-June (lot no. 7978). Wafer-level probing of the 5-bit ADC and S/H circuits was subsequently completed. The April lot yielded several partially functional S/H circuits that exhibited degraded gain, offset, and dc linearity performance. However,

no functional 5-bit ADCs were found among the four wafers processed in the April lot.

During June, Hughes received four additional 5-bit ADC test-bar wafers from TI (lot no. 7978). Wafer-level probing of the 5-bit ADC and one out of four versions of the S/H circuits were completed by the end of the month. No functional 5-bit ADCs were found. Therefore, design verification of the 5-bit ADC chip could not be performed with either of the two lots. However, two functional S/H circuits were located, for a total functional yield of 2%. The functional S/H is the most conservative design version and utilizes HBT devices with 7 x 7 μm^2 emitters and 5 x 5 μm^2 Schottky diodes. The remaining three S/H versions, which utilize smaller 5 x 5 μm^2 square emitters, will be probed in July.

At probe, a number of dc parameters were measured including power supply currents, input offset voltage, gain, and track/hold functionality. The input/output transfer functions of the S/H gate and hold amplifier were measured and a least squares fit routine was used to determine each component's linearity. Wafer-probe data show that the gate and hold amplifier exhibits 9.5 bit (0.14%) dc linearity, which differs significantly from the required and simulated 13 bit (0.012%) performance. The reduced performance can be attributed to poor transistor current gain.

This quarter, a detailed architecture study for the 1.5 Gsps 8-bit ADC design continued. The optimum 8-bit quantizer folding and interpolation architecture was identified. Critical design factors that were considered include optimum dc linearity and temperature stability, input signal distribution, required decoding circuitry, and layout factors.

Detailed circuit simulation of the 8-bit ADC cannot be completed until an accurate model for the overgrowth HBT transistor can be established. Accurate modeling of device parameters including β, junction breakdown voltages and capacitances, and f_T are required if simulation results are to be meaningful. In addition, accurate statistical information concerning V_{be} and β matching is critical for circuit design optimization.

Progress toward completion of the 8-bit ADC mask set is expected to be delayed until an HBT process with stable current gain and reasonable yield can be established. Although the most recent HBT lot has produced a handful of functional S/H circuits, no functional or even partially functional 5-bit ADCs were found. The successful fabrication of this key building block is required to confirm simulated performance and validate the design approach, before detailed design of the 8-bit ADC can be initiated. Therefore, a significant slip in the release of the 8-bit and 12-bit mask sets is expected.

- Device Characterization

  Modeling efforts are on hold until a representative overgrowth lot is received.

- Personnel Assignments

  There have been no changes in personnel.

- Plans for July

  TI will:

  - Run special test to isolate low current gain problems.
  - Continue electrically characterizing the completed lots.
  - Continue Overgrowth Process development.
  - Develop improved n-ohmic metal process.

  Hughes will:

  - Complete wafer-level testing of the remaining three S/H designs.
  - Initiate dynamic testing of the functional S/H circuits.

- Plans for Next Quarter

  Hughes will:

  - Complete wafer-level testing of the remaining three S/H designs on lot 7978.

- Initiate dynamic testing of the functional S/H circuits from lot 7978.
- Complete wafer-level testing of the third test-bar lot expected from TI during August and verify the 5-bit ADC design.
- Dynamically evaluate any 5-bit ADC and S/H circuits from the August lot.
- Initiate detailed characterization of HBT devices from August lot, if representative of processing goals.
- Initiate detailed design of 8-bit ADC if stable HBT process with acceptable current gain is established.

- Unofficial DARPA Financial Status Report

  This is the financial status as of 30 June 1988:

	Funds Authorized	Funds Spent	Amount Billed	Amount Received
FY88	$1,330,000	$1,078,850	$1,028,850	$957,967

Contract Number: N00014-87-C-0314
Contract Title: GaAs Heterojunction Device Based A/D
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